IN THE CLAIMS

Please cancel claims 4, 6-8, 10, 14, 16-17, 20, 22, 32, 34, 39, 44, and 53 without prejudice.

Please amend the following of the claims which are pending in the present application:

1. (Currently amended) A method for fabrication of a semiconductor device on substrate, the semiconductor device having a plurality of layers[[;]] , the method including ~~the steps~~:

(a) applying a seed layer of a thermally conductive metal to a first surface of the semiconductor device;

(b) electroplating a relatively thick layer of the thermally conductive metal on the seed layer, the thermally conductive metal of sufficient thickness to provide a heat sink; and

(c) removing the substrate.

2. (Original) A method as claimed in claim 1, wherein the first surface is coated with an adhesion layer prior to application of the seed layer.

3. (Currently amended) A method as claimed in claim 1 ~~or claim 2~~, wherein the seed layer is patterned with photoresist patterns before the electroplating step

(b), and the electroplating of the relatively thick layer is between the photoresist patterns.

4. (Cancelled)

5. (Currently amended) A method as claimed in ~~any one of claims 1 to 4~~ claim 1, wherein between steps (b) and (c) there is performed the additional step of annealing the layers to improve adhesion, and the photoresist patterns are of a height in the range 15 to 500 micrometers, a thickness in the range 3 to 500 micrometers, and a spacing in the range of 200 to 2,000 microns.

6-8. (Cancelled)

9. (Currently amended) A method as claimed in ~~any one of claims 1 to 8~~ claim 1, wherein the seed layer is electroplated in step (b) without patterning, patterning being performed subsequently by photoresist patterning and then wet etching.

10. (Cancelled)

11. (Currently amended) A method as claimed in claim [[9]] 3, wherein patterning is by laser beam micro-machining of the relatively thick layer.

12. (Currently amended) A method as claimed in ~~any one of claims 3 to 11~~ claim 3, wherein the relatively thick layer is of a height no greater [[that]] than the photoresist height.

13. (Currently amended) A method as claimed in ~~any one of claims 3 to 11~~ claim 3, wherein the relatively thick layer of thermally conductive metal is electroplated to a height greater than the photoresist and is subsequently thinned, thinning being by polishing or wet etching.

14. (Cancelled)

15. (Currently amended) A method as claimed in ~~any one of claims 1 to 14~~ claim 1, wherein after step (c) there is included an extra step of forming on a second surface of the semiconductor device a second ohmic contact layer, the second ohmic contact layer being selected from the group consisting of: opaque, transparent, and semi-transparent, the second ohmic contact layer being one of blank and patterned, bonding pads being formed on the second ohmic contact layer.

16-17. (Cancelled)

18. (Currently amended) A method as claimed in ~~any one of claims 1 to 14~~ claim 1, wherein after step (c) ohmic contact formation and subsequent process steps are carried out, the subsequent process steps including deposition of wire bond pads.

19. (Currently amended) A method as claimed in claim [[18]] 15, wherein the exposed second surface is cleaned and etched before the ohmic contact layer is deposited, the second ohmic contact layer not covering the whole area of the second surface.

20. (Cancelled)

21. (Currently amended) A method as claimed in ~~any one of claims 15 to 20~~ claim 15, wherein after forming the second ohmic contact layer there is included testing of the semiconductor devices on the epitaxial layers, and separating the layers into individual devices.

22. (Cancelled)

23. (Currently amended) A method as claimed in ~~any one of claims 1 to 22~~ claim 1, wherein the semiconductor devices are fabricated without one or more selected from the group consisting of: lapping, polishing and dicing.

24. (Currently amended) A method as claimed in ~~any one of claims 1 to 23~~ claim 1, wherein the semiconductor device comprises a plurality of epitaxial layers, a first ohmic contact layer being on a first surface of the epitaxial layers remote from the substrate; the first ohmic contact layers being on p-type layers of the epitaxial layers.

25. (Currently amended) A method as claimed in [[any]] claim [[22]] 24, wherein the second ohmic contact layer is formed on n-type layers of the expitaxial layers.

26. (Currently amended) A method as claimed in ~~any one of claims 1 to 14~~ claim 1, wherein after step (c), dielectric films are deposited on the epitaxial layers and openings are cut in the dielectric films and second ohmic contact layer and bond pads deposited on the epitaxial layers.

27. (Currently amended) A method as claimed in ~~any one of claims 1 to 14~~ claim 24, wherein after step (c), electroplating of a thermally conductive metal on the semiconductor device is performed.

28. (Currently amended) A method as claimed in ~~any one of claims 24 to 26 and claim 27 when appended to any one of claims 24 to 26~~ claim 27, wherein the

thermally conductive metal comprises copper and the epitaxial layers comprise multiple GaN-related layers.

29. (Currently amended) A semiconductor device comprising epitaxial layers, first ohmic contact layers on a first surface of the epitaxial layers, a relatively thick layer of a thermally conductive metal on the first ohmic contact layer to form a heat sink, and a second ohmic contact layer on a second surface of the epitaxial layers, an adhesive layer on the first ohmic contact layer between the first ohmic contact layer and the relatively thick layer[[;]], the relatively thick layer being applied by electroplating.

30. (Previously presented) A semiconductor device as claimed in claim 29, wherein there is a seed layer of the thermally conductive metal, applied to the adhesive layer.

31. (Currently amended) A semiconductor device as claimed in ~~any one of claims 29 and 30~~ claim 29, wherein the relatively thick layer is at least 50 micrometers thick, and the second ohmic contact layer is a thin layer in the range of from 3 to 500 nanometers.

32. (Cancelled)

33. (Currently amended) A semiconductor device as claimed in ~~any one of claims 29 to 32~~ claim 29, wherein the second ohmic contact layer is selected from the group consisting of: opaque, transparent, and semi-transparent, and includes bonding pads.

34. (Cancelled)

35. (Currently amended) A semiconductor device as claimed in ~~any one of claims 29 to 34~~ claim 29, wherein the thermally conductive metal is copper and the epitaxial layers comprise multiple GaN-related epitaxial layers.

36. (Currently amended) A semiconductor device as claimed in ~~any one of claims 29 to 35~~ claim 29, wherein the semiconductor device is selected from the group consisting of: a light emitting device, and a transistor device.

37. (Previously presented) A semiconductor device comprising epitaxial layers, a first ohmic contact layer on a first surface of the epitaxial layers, an adhesive layer on the first ohmic contact layer, and a seed layer of a thermally conductive metal on the adhesive layer.

38. (Currently amended) A semiconductor device as claimed in claim 37, further ~~including~~ comprising a relatively thick layer of the thermally conductive

metal on the seed layer, the relatively thick layer acting as a heat sink, and a second ohmic contact layer on a second surface of the epitaxial layers, the second ohmic contact layer being a thin layer in the range of from 3 to 500 nanometers.

39. (Cancelled)

40. (Currently amended) A semiconductor device as claimed in ~~any one of claims 37 to 39~~ claim 37, wherein the second ohmic contact layer comprises bonding pads and is selected from the group consisting of: opaque, transparent, and semi-transparent.

41. (Currently amended) A semiconductor device as claimed in ~~any one of claims 37 to 40~~ claim 37, wherein the thermally conductive metal comprises copper[[;]], and the epitaxial layers comprise GaN-related layers.

42. (Currently amended) A method of fabrication of a semiconductor device, the method including ~~the steps~~:

(a) on a substrate with a plurality of epitaxial layers comprising multiple GaN-related epitaxial layers, forming a first ohmic contact layer on a first surface of the epitaxial layers;

(b) removing the substrate from the epitaxial layers; and

(c) forming a second ohmic contact layer on a second surface of the epitaxial layers, the second ohmic contact layer having bonding pads formed thereon.

43. (Currently amended) A method as claimed in claim 42, wherein the second ohmic contact layer is selected from the group consisting of: opaque, transparent, and semi-transparent and is one of: blank, and patterned.

44. (Cancelled)

45. (Currently amended) A semiconductor device fabricated by the method of ~~any one of claims 42 to 44~~ claim 42.

46. (Previously presented) A semiconductor device as claimed in claim 45, wherein the semiconductor device is one of: a light emitting device, and a transistor device.

47. (Currently amended) A method for fabrication of a semiconductor device on a substrate, the semiconductor device having a plurality of layers with a device layer[[;]], the method including ~~the steps~~:

(a) electroplating a layer of a thermally conductive material onto a surface of the semiconductor device remote from the substrate and close to the device layer; and

(b) removing the substrate.

48. (Previously presented) A method as claimed in claim 47, wherein the semiconductor device is a silicon-based device.

49. (Currently amended) A method for fabrication of a light emitting device on a substrate, the light emitting device having a plurality of layers with an active layer[[;]], the method including ~~the steps~~:

(a) electroplating a layer of a thermally conductive material onto a surface of the semiconductor device remote from the substrate and close to the active layer; and

(b) removing the substrate.

50. (Currently amended) A method as claimed in ~~any one of claims 47 to 49~~ claim 49, wherein the thermally conductive layer is as a heat sink.

51. (Currently amended) A method as claimed in claim [[50]] 49, wherein the thermally conductive layer is of a thickness in the range of from 3 microns to 300 microns.

52. (Currently amended) A method as claimed in claim ~~50 or claim 51~~ 49, wherein the thermally conductive layer is of a thickness of from 50 to 200 microns.

53. (Cancelled)